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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,509	03/01/2004	Manish K. Ahluwalia	200315654-1	1055
22879	7590	11/24/2008	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				LI, ZHUO H
ART UNIT		PAPER NUMBER		
2185				
			NOTIFICATION DATE	DELIVERY MODE
			11/24/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/790,509	AHLUWALIA, MANISH K.	
	Examiner	Art Unit	
	ZHUO H. LI	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 July 2008.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-23 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application

6) Other: _____.

DETAILED ACTION

Response to Applicant's Appeal Brief

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. The Office action is in responds to the Appeal Brief filed on 7/30/2008, claims 1-23 are pending in the application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 23 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 23 is not limited to tangible embodiments. In view of Applicant's disclosure, in Specification ([0024]), the term "a computer readable medium having a program" is not limited to tangible embodiments (e.g., the computer readable medium include an electronic circuit, a semiconductor memory device, a ROM, a flash memory, an erasable ROM (EROM), a floppy diskette, a compact disk CD-ROM, an optical disk, a hard disk, a fiber optic medium, a radio frequency (RF) link), and intangible embodiment (e.g., the program or code segments can be stored in a computer/processor readable medium or transmitted by a computer data signal embodied in a carrier wave, or a signal modulated by a carrier, over a transmission medium, a computer readable medium may include any medium that can store or transfer information, i.e., software which can transfer signal defined above as carrier waves, and the computer data signal may include any signal that can propagate, i.e., propagate is merely a signal or carrier waves,

over a transmission medium such as electronic network channels, optical fibers, air, electromagnetic, RF links, etc., i.e., software). As such, the claim is not limited to statutory subject matter and is therefore non-statutory. In order to limit to statutory subject matter in the claim limitation, it needs to be clarified “a computer readable storage medium” in the claim and further definition of storage medium or physical medium as defined above, and distinguish the non-statutory subject matter, i.e., transmission medium to transfer propagate signal, in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 8, the limitation, “wherein registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released, and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process”, which it is unclear how to registering is triggered to detect the physical address space is released, when the device has been released.

Claims 2-7 and 9-12 are also rejected because of depending on claim 1 respectively, containing the same deficiency.

The following art rejections are applied from what is best understood of the claim(s) in view of the 112 Second paragraph problems listed above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over (US PAT. 6,907,494 hereinafter Armilli) in view of Browning et al. (US PAT. 6,918,023 hereinafter Browning).

Regarding claim 1, Armilli discloses a computer device (8, figure 3) comprising a processor (10, figure 3), a memory (22, figure 3) coupled to the processor via the system bus (12, figure 3), and program instructions provided to the memory and executable by the processor to track a virtual address space for a process associated with a device connected to the computer device (figure 2 and col. 5 line 66 through col. 6 line 39), and release a physical address space associated with the virtual address space when the device has a connection removed from the computer device (col. 7 lines 32-57, i.e., removing memory module from data processing system). Armilli differs from the claimed invention in not specifically teaching to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, wherein

registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process. However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is set on memory removal process (step 834), i.e., registering is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Arimilli to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available

to the process, is no longer valid for process use, wherein registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claims 2-3, Arimilli discloses the device includes a device, i.e., mapping engine (26, figure 3), which can be mapped to memory, and the virtual address space includes an input/output space (col. 7 lines 58-65).

Regarding claim 4, Arimilli discloses the program instructions are part of a memory management system, which includes a virtual memory data structure associated with the process (col. 6 line 66 through col. 7 line 15).

Regarding claim 5, Arimilli discloses the program instructions execute to register the virtual address space is no longer valid for process use in the virtual memory data structure associated with the process (col. 8 lines 9-26).

Regarding claim 6, Arimilli discloses the program instructions execute to allocate the virtual address space when the process requests physical memory (col. 8 line 51 through col. 9 line 10).

Regarding claim 7, Arimilli discloses the program instructions execute to register that the virtual address space is available for use when the process releases the virtual address space (col. 7 lines 32-57).

Regarding claim 8, Arimilli discloses a computing device (8, figure 3) comprising a processor (10, figure 3), a random access memory (22, figure 3) coupled to the processor via the

system bus (12, figure 3), and program instructions provided to the memory and executable by the processor to deference a virtual address space for a process associated with a removable memory mappable device connected to the computer system (figure 2 and col. 5 line 66 through col. 6 line 39), and release a physical address space associated with the virtual address space when the device has a connection removed from the computer device (col. 7 lines 32-57).

Although Armilli teaches to register that the virtual address space before when the process has released the virtual address space (col. 7 lines 32-42), Armilli differs from the claimed invention in not specifically teaching to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use subsequent to when the physical address space is released, wherein registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process.

However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is set on memory removal process (step 834), i.e., registering is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further

comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Arimilli to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, wherein registering is triggered by detection that the physical address space that was being used by processes associated with the device has been released; and wherein the registering occurs as the physical address space is released and before release of the virtual address space by the process, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claim 9, Arimilli discloses the program instructions execute to un-map the virtual address space in a manner which do not violate semantics for an operating system of the computing device (abstract and col. 11 lines 6-26).

Regarding claim 10, Arimilli differs from the claimed invention in not specifically teaches the operating system is selected from the group of a Unix operating system and a Linux operating system. However, it is old and notoriously well known in the art that kernel is a core of an operating system, a portion of the system that manages memory, files, and peripheral devices,

maintains the time and data, launches applications, and allocates system resources, as defined by *Microsoft Computer dictionary Fifth edition*, furthermore, kernel is defined as an operating system (OS) of the essential part of Unix operating systems, i.e., Linus OS in *On-line Computing Dictionary* (<http://www.instantweb.com/foldoc/foldoc.cgi?query=kernel&action=Search>). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the operating system in the computer system of Arimilli is selected from the group of a Unix operating system and a Linux operating system, because it improves and enhances the flexibility in the computer system.

Regarding claims 11-12, Arimilli discloses the program instructions execute to allow the process to un-map the virtual address space subsequent to the release of the physical address space and to indicate an operation as failed if the process attempts to perform the operation subsequent to registering that the virtual address space is no longer valid for process use (col. 7 lines 17-42).

Regarding claim 13, Armilli discloses a computer device (8, figure 3) comprising a processor (10, figure 3), a memory (22, figure 3) coupled to the processor via a system bus (12, figure 3), the memory including program instructions for maintaining a virtual memory data structure as part of a memory management system, i.e., program provided an address translation mechanism that translates virtual addresses to physical addresses (col. 5 lines 5-53), and means for un-mapping a virtual address space, i.e., processor's move engine (28, figure 3), for a process in a manner which does not violate semantics for an operating system of the computing device when a removable memory mappable device associated with the process is logically disconnected (abstract and col. 7 line 32 through col. 9 line 10, i.e., the processor's move engine

works in conjunction with the associated mapping engine to take the associated memory module offline, read as un-mapping a virtual address space, prior to its physically removal, read as when the removable memory mappable device associated with the process is logically disconnected, such that the memory module can be removed in physical memory without the operating system having to direct and control the reconfiguration of physical memory to accomplish the physical memory change, read as for a process in a manner which does not violate semantics for an operating system of the computing device). Arimilli differs from the claimed invention in not specifically teaching that means for un-mapping the virtual address space for the process that is triggered as a physical address space used by the process is being released. However, Browning teaches a method for invalidating specified pre-translations maintained in a data processing system which maintains decentralized copies of pre-translations, wherein the data processing system comprising a DMA mapping agent to map a virtual buffer to physical address (steps 802-816, figure 8), when a detection on memory removal operation is being process (col. 7 lines 21 through col. 8 line 44), and also defined in figure 8 that determining whether the RPN entry for the virtual memory page is valid (step 824), when flag is set on memory removal process (step 834), i.e., registering is triggered by detection that the physical address space that was being used by process associated with the device is being released, and the virtual memory page is maintained for mapping as defined in step 828, and further comprising the steps of to register by providing an indication in the virtual memory data structure for the process that the virtual address space, previously available to the process, is no longer valid for process use, as defined in steps 824-830 in figure 8, and (step 910, figure 9 and col. 8 lines 58-64, i.e., scan all registered RPN lists and invalidates all entries, including virtual address space, corresponding to real pages

that within the range of memory to be removed), and (col. 8 lines 53-58, i.e., receiving acknowledgement of interrupt from all CPUs and then triggering to register by detecting that real pages that are within range of memory to be removed). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Arimilli in having means for un-mapping the virtual address space for the process that is triggered as a physical address space used by the process is being released, as per teaching of Browning, in order to provide for invalidating pre-translations without the use of locks or semaphores.

Regarding claim 14, Arimilli discloses the program instructions execute to dereference the virtual address space for the process (col. 7 line 43 through col. 8 line 8 line 50, i.e., to perform memory reconfiguration in response to memory module M2 being removed from data processing system).

Regarding claim 15, Arimilli discloses the means for un-mapping the virtual address space includes program instructions, which execute to maintain a representation of an object associated with the process in the virtual memory data structure of the process (col. 8 line 51 through col. 9 line 10, i.e., creating a virtualized physical mapping from the addressable read address space being utilized by operating system into a virtual physical address space).

Regarding claim 16, Browning discloses the means for un-mapping the virtual address space includes program instructions which execute to remove a mapping of the object to physical memory (col. 8 line 45 through col. 9 line 27).

Regarding claims 17-18, Browning discloses the means for un-mapping the virtual address space includes program instructions which execute to register in the virtual memory data structure of the process that the virtual address space associated with the process is not available

for use, and the program instructions execute to set a bit in the region of the virtual memory data structure to indicate that the virtual address space is not available for use (col. 8 line 45 through col. 9 line 27).

Regarding claim 19, the limitations of the claim are rejected as the same reasons as set forth in claim 8.

Regarding claims 20-21, the limitations of the claims are rejected as the same reasons set forth in claims 11-12.

Regarding claim 22, the limitations of the claim are rejected as the same reasons as set forth in claim 1.

Regarding claim 23, the limitations of the claim are rejected as the same reasons set forth in claim 19.

Response to Arguments

Applicant's arguments filed on 7/30/2008 have been fully considered but they are not persuasive.

In respond to Applicant's argument that independent claim 23 recites statutory subject matter because defined definition of the "computer readable medium" defined in Page 7 in specification. It is noted that the definition of the "computer readable medium" in recited section contains alternative meaning, i.e., the computer readable medium can be a physical storage medium as defined with physical memory in lines 14-16 in Page 7, or it can be a transmission medium as defined to transfer any signal that can propagate in lines 16-21". Examiner has

further explained how to limit the claimed limitation to become statutory subject matter in current Office action above. Thus claim 23 is rejected under 35 U.S.C. 101.

In respond to Applicant's argument that the cited reference do not teach, suggest, or render obvious each and every element and limitation for independent claims 1, 8, 19, and 22-23, especially the cited reference do not teach the registering occurs as the physical address space is released and before release of the virtual address space by the process. It is noted that the limitation stated in claims 1 and 8 is unclear how to registering is triggered to detect the physical address space is released, when the device has been released. Examiner took a broadly interpretation to make a rejection based upon the other similar limitation in claims 13, 19, 22, and 23, which registering is triggered to detect the physical address space is released, when the device is being released. According, Browning teaches to determining memory removal in process flag set, i.e., memory is being released or not, after confirmed the RPN entry for the virtual memory page valid by the DMA mapping engine, and if the flag is set, it further perform DMA mapping to remapping corresponding to the virtual memory page, i.e., old physical address space is released before release of the virtual address space, as defined in figure 8, and col. 7 line 21 through col. 8 line 64), so as addressed in the modified rejection above. Thus, claims 1, 8, 19, and 22-23 are rejected by the combination of Arimilli and Browning.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ZHUO H. LI whose telephone number is (571)272-4183. The examiner can normally be reached on Mon - Fri 6:00am - 2:30pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zhuo H Li/
Examiner, Art Unit 2185

/Sanjiv Shah/
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